REMARKS

Claims 1 – 4, 7, 10, 12, 15, 19, 20 – 22, 24 – 33, 52, 53, 55, 60, 63 and 66 have been amended, and claims 23 and 107 – 110 have been canceled. Therefore, claims 1 – 22 and 24 – 106 remain pending in the captioned case. Reconsideration is respectfully requested in light of the following remarks.

Objection to the Specification:

The Examiner objected to the Abstract of Applicants' specification because "extraneous markings (i.e. 'Attorney Docket …')." However, the so-called extraneous markings referred to by the Examiner are part of the page header and are not part of the Abstract itself. The Office does not treat page header and footer information as part of the content or material of the application. The objection to the Abstract is in error and withdrawal thereof is respectfully requested.

The Examiner also objected to the Specification "as failing to provide proper antecedent basis for the claimed subject matter." Specifically, the Examiner asserts that "[t]he computer readable medium in the claims does not appear to be present in Applicant's original specification." Applicants' have amended to the specification to include proper antecedent basis for the claimed computer readable medium based on the subject matter of the original claims, which are considered part of the original disclosure.

Claim objections:

The Examiner objected to claims 1-20, 22-31, 54-57, 63 and 66 for various informalities. Applicants submit that the claims have been amended to overcome these objections. Additionally, Applicants note that the term "ABA" is not an acronym, but instead is a term of art.

Section 101 Rejection:

The Examiner rejected claims 21-33 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claims 21 – 33 have been amended. Withdrawal of the rejection is respectfully requested.

Section 112, Second Paragraph, Rejection:

The Examiner rejected claims 1-20, 24-26, 52-66 and 107-110 under 35 U.S.C. § 112, second paragraph, as indefinite. Specifically, the Examiner rejected claims 1, 7, 10, 20, 24, 52 and 107 as having insufficient antecedent basis for the various phrases. Claims 2-20, 25-26, 53-66 and 108 – 110 were rejected "for further limiting claims 1, 24, 52 and 107 respectively." Claims 1, 7, 10, 20, 24 and 52 have been amended to overcome this rejection and claim 107 has been canceled. Applicants therefore respectfully request removal of the §112, second paragraph, rejection.

Section 102(b) Rejection:

The Examiner rejected claims 21 and 31 under 35 U.S.C. § 102(b) as being anticipated by MacGregor, et al. (U.S. Patent 4,584,640) (hereinafter "MacGregor"). Applicants respectfully traverse this rejection for at least the reasons below.

Regarding claim 21, MacGregor fails to disclose a snapshot mechanism configured to verify a state of k-1 other targeted locations, wherein k is greater than 1. MacGregor teaches a compare and swap instruction for simultaneously swapping 2 values. In MacGregor's system, the status of the two values are read prior to the instruction and during the instruction these locations are checked again to ensure that no change has occurred at these locations before the instruction performs the swap of the two new values.

The Examiner cites, regarding claim 23, column 6, lines 26 – 53 of MacGregor. The cited passage describes MacGregor's read-modify-write cycle (RMC) that ensures in advance that a write can follow a read without relinquishing the bus. At the cited passage, MacGregor also states that a CAS1 instruction (i.e. a compare and swap instruction for a single location) is not appropriate for a doubly-linked list. MacGregor then introduces his CAS2 instruction for double-linked lists.

However, MacGregor fails to teach anything regarding a snapshot mechanism configured to verify a state of k-1 other targeted locations, where k is greater than 1. Instead, MacGregor teaches verifying only to two locations two be swapped. In contrast Applicants claim recites verifying the state of a plurality of locations other than the first targeted location to be updated.

Applicants remind the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, MacGregor fails to disclose **a snapshot mechanism configured to verify a state of k-1 other targeted locations, wherein k is greater than 1**. Therefore, MacGregor cannot be said to anticipate claim 1. Thus, the rejection of claim 21 is not supported by the cited art and removal thereof is respectfully requested.

Section 103(a) Rejection:

The Examiner rejected claims 1-5, 9, 11, 14-17, 23, 24, 26, 29, 30, 52, 53, 55, 57, 60-63, 66, and 107-109 under 35 U.S.C. § 103(a) as being unpatentable over MacGregor as applied to claim 21 above, and further in view of Greenspan et al. (U.S. Patent 6,128,710) (hereinafter "Greenspan"). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 1, MacGregor in view of Greenspan fails to teach or suggest **snapshotting a plurality of application values corresponding to a respective plurality of targeted memory locations to determine whether any of the application values are changed between two successive reads at the targeted memory locations, wherein said snapshotting comprises reading each of the plurality the application values at least twice and comparing each application values across pairs of successive reads.**

The Examiner cites The Examiner cites, regarding claim 23, column 6, lines 26 – 53 of MacGregor. As noted above, the cited passage describes MacGregor's read-modify-write cycle (RMC) that ensures in advance that a write can follow a read without relinquishing the bus. At the cited passage, MacGregor also states that a CAS1 instruction (i.e. a compare and swap instruction for a single location) is not appropriate for a doubly-linked list. MacGregor then introduces his CAS2 instruction for double-linked lists.

MacGregor's system does not involve snapshotting a *plurality* of values that includes *reading each of a plurality of values at least twice* and comparing each value *across pairs of successive reads*. Instead, MacGregor teaches comparing the values in a next and tail pointers of a doubly-linked list to "corresponding stored compare values" (MacGregor, column 8, lines 27-32). Nowhere does MacGregor mention anything regarding reading each of a plurality of values at least twice and comparing the read values across pairs of successive reads, as recited in Applicants' claim.

The Examiner relies on Greenspan to teach the use of application values, but Greenspan, whether considered singly or in combination with MacGregor, fails to teach or suggest anything regarding snapshotting a plurality of application values corresponding to a respective plurality of targeted memory locations, wherein said snapshotting comprises reading each of the plurality the application values at least twice and comparing each application values across pairs of successive reads. Thus, Greenspan fails to overcome MacGregor's deficiency regarding this limitation of claim 1.

Therefore, MacGregor and Greenspan, whether considered singly or in combination, fail to teach or suggest **snapshotting a plurality of application values corresponding to a respective plurality of targeted memory locations to determine whether any of the application values are changed between two successive reads at the targeted memory locations, wherein said snapshotting comprises reading each of the plurality the application values at least twice and comparing each application values across pairs of successive reads**, as recited in Applicants' claim 1.

MacGregor in view of Greenspan further fails to teach or suggest **updating a first application value corresponding to a first targeted memory location only if the snapshotting indicates that the plurality of application values remain unchanged between two successive reads at the targeted locations, where the first targeted location is distinct from the plurality of targeted locations**. Instead, MacGregor teaches comparing the values in a next and tail pointers of a doubly-linked list to corresponding stored compare values and if each compare value is the same as its corresponding test value, the swap values are swapped for the corresponding values in the next and tail pointers (MacGregor, column 8, lines 27-33). Nowhere does MacGregor, whether considered singly or in combination with Greenspan, teach or suggest anything regarding updating a first value only if a plurality of other application values at locations distinct from the first value being updated remain unchanged between two successive reads.

For at least the reasons above, the rejection of claim 1 is not supported by the cited art and removal thereof is respectfully requested. Similar remark also apply to claim 52.

The Examiner rejected claims 32 and 33 under 35 U.S.C. § 103(a) as being unpatentable over MacGregor in view of Yeh et al. (U.S. Publication 2003/0105943) (hereinafter "Yeh"), claim 22 as being unpatentable over MacGregor in view of Bonola (U.S. Publication 2003/0065892), claims 6-8, 20 and 54 as being unpatentable over MacGregor and Greenspan in further view of Bonola. Applicants respectfully traverse

the rejection of these claims for at least the reasons presented above regarding their respective independent claims.

Regarding both the §102 and §103 rejections above, Applicants also assert that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the rejections have been shown to be unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/6000-31700.

Also enclosed herewith are the following items:

☐ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,

/Robert C. Kowert/

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